

REMARKS

Claims 1-5, 7-10 and 19-21 are pending. Claim 1 has been amended to include the limitations of claim 19, and claim 19 has been cancelled. Claims 11-18 were previously cancelled with the prior response. Reconsideration of the application is respectfully requested for at least the following reasons.

I. REJECTION OF CLAIM 20 UNDER § 112, SECOND PARAGRAPH

Claim 20 was rejected under 35 U.S.C. § 112, second paragraph as being indefinite. Withdrawal of the rejection is respectfully requested for at least the following reasons.

The Office Action stated that there appeared to be an overlap of data being stored in the two memories as recited in claim 20. Amended claim 20 discloses a first memory coupled with the bus interface system and the security system for storage of outgoing data from the host system prior to encryption and incoming data to the host system after decryption, and a second memory coupled with the media access control system and the security system for storage of incoming data from the network prior to decryption and outgoing data to the network after encryption. By distinguishing between the outgoing and incoming data for each memory, applicants believe claim 20 to be definite. Withdrawal of the rejections is therefore respectfully requested.

II. REJECTION OF CLAIMS 1-5, 8, 9, 19 AND 20 UNDER § 103(a)

Claims 1-5, 8, 9, 19 and 20 were rejected under 35 U.S.C. §103(a) as being anticipated by U.S. Patent Publication No. 2004/0062267 (Minami) in view of U.S. Patent Publication No. 2001/0014936 (Jinzaki). Withdrawal of the rejection is respectfully requested for at least the following reasons.

i. One of ordinary skill in the art would not have been motivated to combine Minami with a FIFO as taught by Jinzaki .

Claim 1 relates to a network interface system comprising a security system having first and second processors for encrypting outgoing data, wherein the first and second processors each comprise pipelines for ESP encryption, ESP authentication, and AH authentication. The network interface system comprises ***a transmit output data flow controller configured to control the flow of encrypted data from the first and second processors to the memory system in the same order as the order in which the data was read from the memory system***. The Office Action states that Minami discloses the above highlighted feature in combination with Jinzaki disclosing a FIFO throughout the reference. However, one of ordinary skill would not have combined a FIFO memory as taught in Jinzaki with the teachings of Minami for IPsec processing.

In particular, Jinzaki teaches away from implementing a FIFO memory together with first and second processors each comprising pipelines for ESP encryption, ESP authentication, and AH authentication. For example, Jinzaki states in paragraph [0222] that ***in more complicated packet labeling where IPsec exists . . . “use of a simple FIFO memory as shown in Fig. 33 is insufficient, and a system where a plurality of stream processors run with pipeline processing become necessary.”*** Thus, because Minami utilizes IPsec processing, one of ordinary skill in the art would not have combined the teachings of Jinzaki with Minami.

Additionally, because claim 1 also discloses that first and second processors for encrypting outgoing data each comprise pipelines (for ESP encryption, ESP authentication, and AH authentication), ***one of ordinary skill in the art would not be motivated to combine the teachings of Jinzaki with Minami*** in order to implement a transmit output data flow controller configured to control the flow of encrypted data from a first and a second processor to the memory system in the same order as the order in which the data was read from a memory system, as recited in claim 1. For example, Jinzaki teaches to replace a FIFO memory with using “a system where a plurality of

stream processors run with pipeline processing.” Thus, because claim 1 discloses that the processors comprise pipelines, one of ordinary skill in the art would not have combined pipelining together with a FIFO memory as taught in Jinzaki. Withdrawal of the rejection is therefore respectfully requested.

- ii. ***Neither Minami nor Jinzaki teach or suggest a transmit output data flow controller configured to control the flow of encrypted data from a first and a second processor to a memory system in the same order as the order in which the data was read from the memory system, as recited in claim 1.***

Minami in view of Jinzaki fail to teach a transmit output data flow controller configured to control the flow of encrypted data from the first and second processors to the memory system ***in the same order as the order in which the data was read from the memory system, as recited in claim 1.*** Minami teaches a security system comprising two parallel and identical encryption engines. (See, par. [1746]). Packets are transferred from a memory to the security system, where the encryption engines are “serviced in alternating order”. (See, par. [1746]). Once serviced, the encrypted packet is written back ***to the same memory location that the source packet came from.*** (See, par. [1745]). Therefore, as taught by Minami, after encryption, packets are written to a memory ***location based upon the location from which they were read.*** Minami does teach that packets are presented in the same order as they were presented to the encryption engine, although this is different from claim 1. In contrast, claim 1 relates to a transmit output data flow controller configured to write data to a memory location ***based upon the order in which it was read.*** Jinzaki does not remedy the deficiency by discussing FIFO memory for synchronizing an input and an output speed, and (as discussed above) Jinzaki teaches away from using such FIFO memory with pipeline processing. No teaching or suggestion is given to control output data flow ***to a memory*** by a controller based upon the order in which it was read. Therefore, Minami in view of Jinzaki fail to teach over the transmit output data flow controller recited in claim 1. Withdrawal of the rejection is therefore respectfully requested.

Claims 2-5, 7-10 and 19-21 depend upon claim 1 and add further limitations thereto. Because claim 1 is nonobvious over the cited art, claims 2-5, 7-10 and 19-21 are also believed nonobvious. Accordingly, withdrawal of the rejection is respectfully requested.

III. CONCLUSION

For at least the above reasons, the claims currently under consideration are believed to be in condition for allowance.

Should the Examiner feel that a telephone interview would be helpful to facilitate favorable prosecution of the above-identified application, the Examiner is invited to contact the undersigned at the telephone number provided below.

Should any fees be due as a result of the filing of this response, the Commissioner is hereby authorized to charge the Deposit Account Number 50-1733, AMDP751US.

Respectfully submitted,
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